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(54) A system for interrupting a transmitter output wave

System zur Unterbrechung der Ausgangswellen eines Senders

Système pour interrompre l'onde de sortie d'un émetteur

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- **PATENT ABSTRACTS OF JAPAN vol. 10, no. 319 (E-450)(2375) 30 October 1986 & JP-A-61 128 654**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a modulator circuit which suppresses generation of spurious frequency spectrum on controlling ON and OFF of the modulated transmittal wave.

Description of the Related Art

In a time division communication system or a frequency division communication system in mobile communication, there is known a system which transmits the signal only when a voice signal is present. In view of simplifying the control of transmitter in such system or a time division communication system, a system for controlling ON and OFF of the modulated output wave with a switch circuit has been used. In this case, momentary transition of ON and OFF of the modulated output signal generates spurious frequency spectrum. A burst control signal of this case is shown in Fig. 2(a), and a spurious pulse frequency generated in the transmittal output signal is shown in Fig. 2(b). Since the other communication system is interfered by this spurious frequency, it is essential to suppress generation of this spurious frequency spectrum.

As a method of suppressing such spurious frequency spectrum, as shown in Fig. 1, a carrier is modulated in the modulator 62 by an input pulse signal whose frequency band is limited to the base band frequency by a low-pass filter 61, and the modulated signal is interrupted by a switch circuit 63 controlled by the burst control signal conforming to the allocated time so as to generate a transmittal signal burst. Otherwise, it is also possible to interrupt the carrier input to the modulator 62 according to the burst control signal, instead of using the switch 63. In this circuit structure, the spurious generated on the transition is reduced by slowing the transition of individual input pulses, resulting in reduced spurious wave generation in the vicinity of carrier frequency. However, in any case, spurious frequency spectrum is generated in the transmittal frequency band momentarily on the ON/OFF transitions of the transmittal signal.

The spectrum in the transmittal frequency band generated by the input signal pulses is attenuated typically conforming to the curve of $S(f) = (\sin x/x)^2$ around the carrier frequency f_o as shown by "a" in Fig. 3. The spurious frequency spectrum generated on ON/OFF transitions of modulated transmittal signal includes a wide frequency component as shown by "b". Therefore, it causes a serious interference into the other communication systems.

In order to eliminate such spurious frequency spectrum, a band-pass filter 64, for example, has been employed in the prior art in the successive stage of switch 63 as shown in Fig. 4, where the parts like those in Fig. 1 are designated by the like numerals. However, even when such band-pass filter 64 is employed, the spurious frequency spectrum in the pass-band of band-pass filter 64 cannot be eliminated. Moreover, in a mobile communication system, a comparatively low speed data is generally transmitted, and therefore a narrow band-pass filter 64 is used, there is a problem in that an insertion loss becomes large even though the spurious frequency spectrum outside the pass-band can be eliminated.

The modulator 62 explained above is usually formed with a multi-phase phase-modulator or quadrature amplitude phase modulator. Therefore, the modulated signal includes a large change in its amplitude, namely amplitude change of envelope of the modulated signal. Accordingly, there is a moment that the envelope becomes zero, and there has been proposed a method that the spurious frequency spectrum is suppressed by controlling ON and OFF of the modulated signal on this moment. (For example, the U.S. Patent No. 4,644,531 proposed by the inventor of the present invention.) In this method, for example, a same sign which is opposite to the sign immediately before the rise of the burst control signal is continuously given to at least two bits immediately after the rise of the burst control signal, and thereafter the signal is inverted. Or, the sign of at least two bits immediately before the fall of the burst control signal is set opposite to the sign of the preceding bits, and the sign is then inverted immediately after the fall of the burst control signal. Thereby, the signal is controlled ON and OFF at the moment at which the amplitude of the modulated signal becomes zero, and the spread of the spurious frequency band generated thereby can be reduced.

Meanwhile, since the modulated signal whose amplitude does not become zero receives less influence of nonlinearity distortion of the amplifier, the amplifier can be simply structured as well as reduced power consumption can be realized. Accordingly, this method provides a merit of realizing reduction in size of a mobile station in the mobile communication system, and is preferably employed. An example circuit is hereunder explained.

Fig. 5 is a block diagram of an offset 4-phase PSK (Phase Shift Keying) modulation circuit of a prior art. In this figure, numeral 71 designates a 4-phase phase-modulation circuit; 72, a phase shifter for delaying an input signal pulse for a 1/2 bit period; 73, a serial/parallel converting circuit; 74 and 75, low-pass filters; 76 and 77, modulator units each formed with, for example, a balanced mixer; 78, a combiner; 79, a phase shifter for shifting the carrier for /2; 80, a carrier oscillator; and 81, a switch.

An input data is converted to parallel data I and Q by serial/parallel converter 73, and the Q channel output data is shifted for 1/2 bit by phase-shifter 72. The switch 81 is controlled by a burst control signal and thereby the carrier applied to the modulator units 76 and 77 is con-

trolled ON and OFF. When the switch 81 becomes conductive, the carrier from the carrier generator 80 is applied to the modulator units 76 and 77; and the modulated signals, as the respective outputs, are summed in the combiner 78 to become a transmittal signal. When the switch 81 opens, the transmittal signal is cut. Fig. 6 (a) and Fig. 6(b) respectively show modulating signals input to the modulator units 76 and 77 through the low-pass filters 74 and 75 of the I channel and Q channel. Since these signals are shifted by 1/2 bit period with each other, the transmittal signal combined by the combiner unit 78 is shown in Fig. 6(c). Namely, the modulated transmittal signal has a small change in amplitude and does not include any moment at which the amplitude becomes zero.

Fig. 7 is a block diagram of an FSK (Frequency Shift Keying) circuit of the prior art. Numerals 84 and 85 designate low-pass filters; 86 and 87, modulator units each formed, for example, with a balanced mixer; 88, a combiner; 89, a $\pi/2$ phase-shifter; 90, a carrier oscillator; 91, a switch; 92, a serial/parallel converting circuit; 93, an quadrature amplitude phase modulation circuit; and 94, a logic processing circuit.

An input data is converted to parallel data I and Q by the serial/parallel converting circuit 92, applied to the logic processing circuit 94, and then converted to phase-component signals $\cos\phi$ and $\sin\phi$. These phase-component signals $\cos\phi$ and $\sin\phi$ are applied to the modulator unit 93 so as to be quadrature-modulated. Thereby, an FSK-modulated signal is output.

A $\pi/4$-shift QPSK (Quadrature Phase Shift Keying) signal can be obtained by providing a mapping circuit (not shown in the figure) in place of the logic processing circuit 94, thus, after being logic-processed without changing the phase by 180 degrees the data is input to the modulator unit 93. The amplitude of thus modulated signal does not become zero. Therefore, the ON/OFF control of the modulated output signal by these modulation systems causes the following problems. Namely, as described above, the phase-modulated signal and quadrature amplitude phase modulated signal, each of which largely changes the envelope of the modulated signal on the transition of input signal, can be made zero in the amplitude, on ON/OFF of the modulated signal by logical processing of the input pulse signal, accordingly generation of spurious frequency spectrum can be suppressed. However, as mentioned above, in the modulation circuit shown in Fig. 5 or Fig. 7, since the modulated signal output has no moment at which the envelope becomes zero, it is inevitable that the widely spreading spurious frequency spectrum is generated by the ON/OFF transitions of modulated signal.

In order to eliminate such disadvantage, it has been proposed that the input data is previously grouped as a burst, namely as a group of pulse train, transitions of leading edge and trailing edge are dulled by a filter. However, in such a communication system that requires a sufficient time is between the burst periods, the ON/OFF control can be carried out during the pause period between the bursts. But, since the pause period becomes longer and thereby transmission efficiency is lowered, such a method is often difficult to be applied to the mobile communication system.

Features known previously are set out in the preamble of claim 1.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide circuit configurations and methods which allow interruption and resume of a phase-modulated or frequency-modulated transmittal wave, without emitting spurious frequency spectrum at the transitions of interrupting and resuming the transmittal wave.

It is another object of the present invention to provide circuit configurations and methods which allow a shortest guard period between the bursts.

A transmitter according to the present invention is defined in claim 1.

The above-mentioned features and advantages of the present invention, together with other objects and advantages, which will become apparent, will be more fully described hereinafter, with reference being made to the accompanying drawings which form a part hereof, wherein like numerals refer to like parts throughout.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a partial block diagram of a prior art circuit configuration of a transmitter;

FIG. 2 shows generation of spurious waves on ON/OFF of transmittal signal;

FIG. 3 shows frequency spectrum output from the prior art transmitter;

FIG. 4 a partial block diagram of another prior art circuit configuration of a transmitter;

FIG. 5 shows a block diagram of a prior art circuit configuration for an offset four-phase PSK;

FIGs. 6 show waveforms in an offset four-phase PSK;

FIG. 7 shows a block diagram of a prior art circuit configuration for an FSK;

FIG. 8 shows a principle block diagram of the present invention;

FIG. 9 shows a block diagram of a first preferred embodiment of the present invention for operating on the offset four-phase PSK;

FIGs. 10 show waveforms in the first preferred embodiment shown in FIG. 9;

FIG. 11 shows a block diagram of a second preferred embodiment of the present invention for operating on the four-phase PSK;

FIGs. 12 show a guard period in the first and second preferred embodiments of the present invention;

FIG. 13 shows a block diagram of a third preferred embodiment of the present invention for operating

on the FSK;

FIG. 14 shows a block diagram of a logic processing circuit employed in the FIG. 13 third preferred embodiment of the present invention;

FIG. 15 shows a block diagram of a fourth preferred embodiment of the present invention for operating on the $\pi/4$ shift quadrature PSK;

FIG. 16 shows an explanation of the $\pi/4$ shift quadrature PSK;

FIG. 17 shows another explanation of the $\pi/4$ shift quadrature PSK;

FIG. 18 shows a time relation of outputs from a mapping circuit;

FIG. 19 shows an explanation of signal points of the $\pi/4$ shift quadrature PSK; and

FIG. 20 shows a block diagram of a fifth preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 8 is a principle block diagram of the present invention. An input signal, which is a serial baseband signal, is converted to parallel data by an input signal processing circuit 5 and is then input, as signals I' and Q' , to a modulating circuit 1 after being data-processed therein corresponding to the required type of the modulation. The modulating circuit 1 is a widely used quadrature amplitude phase modulation circuit and can selectively conduct a first mode modulating operation, for example, an offset QPSK or FSK in which the amplitude does not become zero in any moment, or a second mode modulating operation, for example, a 2-phase FSK or 4-phase PSK in which the amplitude becomes zero in a certain moment, depending on the type of the input data I' and Q'. The input signal processing circuit 5 further comprises first switch means 2-1 for switching the type of the input data, I' and Q' , for the two types of modulation modes depending on the instruction of controller 3. Functions of the switch means 2-1 are as follow:

(a) The signals I' and Q' or the either one is switched so that an output of the modulating circuit 1 is 100% amplitude-modulated or the phase is modulated in 180 degrees inversion, and as a result the amplitude modulation having a moment at which the amplitude becomes zero is carried out.

(b) In case the modulation unit of modulating circuit 1 (21 and 22, or 41 and 42 described later) is a cosine type (balanced type diode mixer, etc.), a zero output (for example, grounded) of signal I' or Q' makes the output of the modulation unit zero.

(c) In stead of the signal I' or Q' being not input from the input signal processing circuit 5, an output of the modulation unit is set to zero or phase-inverted by opening the input terminal or inputting a predetermined voltage thereto. This switch means 5 is embodied with a simple switch or a wired logic circuit.

The modulated transmittal signal from the modulating circuit 1 is ON/OFF-controlled depending on the instruction of controller 3 by second switch means 2-2, by the use of the function of first switch means 2-1 or by second switch means 2-2 which cuts off an output of the local oscillator or the modulated transmittal signal of the modulating circuit 1.

Interruption of this modulated transmittal signal is switched in such a moment that the amplitude is essentially zero, after the modulated transmittal signal is switched to the second modulation mode from the first modulation mode by the first switch means 2-1. Moreover, after the modulated transmittal signal of the second modulation mode is resumed by the second switch means 2-2 on such a moment that the amplitude of the modulated transmittal signal becomes zero, the first modulation mode is resumed by the first switch means 2-1.

At first, an input method for the offset 4-phase PSK is described below as a first preferred embodiment and those of the other modulation methods are explained as a second and successive preferred embodiments.

Fig. 9 is a block diagram of the first preferred embodiment of the present invention in which a signal modulated by the offset 4-phase PSK is transmitted. In this figure, the numeral 11 designates a modulating circuit; 12, a first switch; 13, a switch control circuit; 14, a serial/parallel converting circuit; 15, a shift circuit; 20, a combiner; 21 and 22, modulator units each formed, for example, with a well-known balanced mixer; 23 and 24, low-pass filters; 25, a phase shifter; 26, a carrier oscillator; and 27, a second switch.

The input data is converted to I and Q channel parallel data by the serial/parallel converting circuit 14. The I channel data is dulled by the low-pass filter 23 and is then applied to the modulator unit 21. The Q channel data is delayed for a 1/2 bit period by the shift circuit 15, and is applied through switch 12 to the low-pass filter 24, where the pulse shape of data signal is dulled, and is applied to the modulator unit 22. The modulating circuit 11 has substantially the same structure as the 4-phase phase modulating circuit 71 of the prior art shown in Fig. 5. The carrier signal supplied from the carrier oscillator 26 is applied to the phase shifter 25 and concurrently applied to the modulator unit 21 after being delayed by $\pi/2$ by the phase shifter 25. Therefore, the carriers having phase difference of $\pi/2$ are modulated and are summed in the combiner 20 to become a transmittal signal. On the other hand, the modulating signal data to be input to the modulator units 21 and 22 are caused to have a phase difference therebetween by a 1/2 bit period by the shift circuit 15. As a result, the modulated signal combined by the combiner 20 does not have a moment at which the amplitude, namely the envelope, becomes zero. For the ON/OFF control of the modulated signal according to a burst control signal input to the switch control circuit 13, at first the switch control circuit 13 opens the first switch 12. Thereby, opera-

tion of the modulation circuit 11 is switched from the offset 4-phase QPSK operation to the 2-phase PSK operation. As is well known, the 2-phase PSK signal includes a zero-amplitude moment, because, at the same time its amplitude is 100 % amplitude modulated. On the moment at which the amplitude becomes zero, the second switch 27 is turned ON or OFF. For interrupting the modulated signal, the second switch 27 is opened so as to discontinue the carrier signal applied to the modulator units 21 and 22. Thereby, the modulated signal output from the combiner 20 is cut. For resuming the modulated signal, the second switch 27 is closed so as to apply the carrier signal to the modulator units 21 and 22, and respective modulated output signals are summed by the combiner 20 to become the modulated transmittal signal.

Figs. 10 conceptionally show waveforms for explaining operations of the first preferred embodiment described above. Fig. 10(a) and Fig. 10(b) respectively show the modulated input data to be applied through the I channel and Q channel low-pass filters 23 and 24 to the modulator units 21 and 22. Envelopes of the modulated output signals applied to the combiner 20 from the modulator units 21 and 22, respectively, have a phase difference between each other a half of one bit period of the input data, namely T/2, and as conceptionally shown in Fig. 10(c), there is no moment at which amplitude of the combined modulated signal becomes zero. For turning ON and OFF the modulated signal to be transmitted in accordance with the burst control signal, the control circuit 13 instructs the first switch to open at the time t1 at which the Q channel modulator-input signal becomes zero as shown in Fig. 10(b). Thereby, as indicated by a dotted line of Fig. 10(b), the Q channel becomes vacant, thus the modulated signal output from the combiner unit 20 becomes the 2-phase PSK modulated signal only of the I channel. When the modulation is carried out for the 2-phase PSK in accordance with the input signals "1" and "0" alternately, the amplitude of the modulated signal is modulated by 100 %; accordingly, its amplitude becomes zero at the moments t2 and t3. When the second switch 27 is opened at the time t2 at which the amplitude becomes zero as shown in Fig. 10(e), the carrier wave applied to the modulators 21 and 22 from the carrier oscillator is discontinued, thus the modulated transmittal signal is cut. For resuming the burst, at first the second switch 27 is closed at the time t3 at which amplitude of the 2-phase PSK signal becomes zero, so as to apply the carrier to the modulator units 21 and 22 from the carrier oscillator 26. In this case, since the first switch 12 is kept opened, the modulating circuit 11 is conducting the 2-phase PSK operation. Next, at the time t4 at which the Q channel modulator input becomes zero, the first switch 12 is closed so that the modulating circuit 11 returns to the offset 4-phase QPSK operation. Accordingly, the period from time t1 to t4 of the data transmitted is defined as a guard period G as shown with the envelope of the transmittal signal shown in Fig.10(f). This guard period G can be set as short as about 1 - 2 bits. At the times t2 and t3, at which the 100% modulated amplitude becomes zero, the spurious frequency spectrum generated on the ON/OFF transitions of the modulated transmittal signal can be suppressed. Though in the first preferred embodiment shown in Fig. 9, the second switch 27 interrupts the carrier wave signal to be input to the modulator units 21 and 22; accordingly, the similar function can be achieved with a structure that the second switch 27 is located (not illustrated) in series to the output of the combiner 20 so as to turn ON and OFF the modulated transmittal output wave.

Fig. 11 is a block diagram of a second preferred embodiment of the present invention. The parts like those in Fig. 9 are designated by the like numerals. Only different in the second embodiment from the first embodiment is that the first switch 12 is replaced with a transfer type switch 12a. Namely, in the first preferred embodiment the Q channel data is disabled by the first switch 12 to realize a 2-phase PSK operation in the modulating circuit 11; however, in the second preferred embodiment, a transfer switch 12a is provided, in place of the ON/OFF switch 12 to apply the I channel data, instead of the Q channel data shifted by T/2, to the Q channel modulator unit 22. In other words, at the time t1 of Fig. 10, the Q channel data to be input to the modulator unit 22 is switched to the I channel data and it is then returned to the Q channel data at the time t4. Accordingly, the modulated input data of I channel is input to both the modulator units 21 and 22 during the period from time t1 to t4, so as to force the modulating circuit 11 to operate the 2-phase PSK modulation like in the case of the first preferred embodiment. Therefore, the modulated signal, combined by the combiner 20 and then transmitted, is 100% amplitude-modulated by the pulses of "1" and "0". On the times t2, and t3 at which the amplitude becomes zero, the modulated transmittal signal is turned ON and OFF according to ON/OFF of the carrier by the second switch 27, or direct ON/OFF of the transmittal signal output from the combiner unit 20by a switch which is not shown in the figure.

Figs. 12 are diagrams for explaining the guard period. Fig. 12(a) indicates I channel data; Fig. 12(b), Q channel data respectively of the first preferred embodiment; Fig. 12(c), Q channel data of the second preferred embodiment; and Fig. 12(d) indicates ON/OFF states of the modulated signal by the second switch 27. Here, a three-bit period of I channel is the guard period between the data bursts. Namely, in the first preferred embodiment, as shown in Fig. 12(b), the two bits of Q channel data are vacant, during which the 2-phase PSK is provided by the I channel data. In the second preferred embodiment, as shown in Fig. 12(c), a 2-phase PSK is carried out by inserting the I channel data in place of the Q channel data. Thus, the modulated signal becomes ON and OFF at the times at which the amplitude becomes zero, as shown in Fig. 12(d).

Fig. 13 is a block diagram of a third preferred embodiment of the present invention which is applied to an FSK modulating circuit. In this figure, the numeral 31 designates a modulating circuit; 32, a first switch circuit; 33, a control circuit; 34, a serial/parallel converting circuit; 35, a logic processing circuit; 40, a combiner; 41 and 42, modulator units; 43 and 44, low-pass filters; 45, a phase shifter; 46, a carrier oscillator; and 47, a second switch circuit. The modulating circuit 31, serial/parallel converting circuit 34 and logic processing circuit 35 in the third preferred embodiment respectively correspond identically to the modulator 93, serial/parallel converting circuit 92 and logic processing circuit 94 of the prior art FSK modulating circuit shown in Fig. 7. In this third preferred embodiment, the first switch 32 consisting of two transfer switches is additionally connected as shown in FIG. 3. Namely, when contacts "a" and "a'" are selected, the inputs to the low-pass filters 43 and 44 become the I' and Q' channel signals from the serial/parallel converting circuit 34. When the contacts "b" and "b'" are selected, the inputs are switched respectively to the output signals I and Q from the serial/parallel converting circuit 34. When the input to the modulating circuit 31 is connected to the contacts "a" and "a'", the FSK signal by the quadrature modulation is transmitted from the combiner 40 as in the case of the prior art of Fig. 7. This FSK signal does not have a moment at which the amplitude becomes zero. For turning ON and OFF the modulated signal according to the burst control signal, at first the switch control circuit 33 instructs the first switch circuit 32 to be switched to the contacts "b" and "b'", for example, at the time t1. At this time, since the modulating circuit 31 conducts the 4-phase PSK operation, the output signal is 100% amplitude-modulated so as to have a moment at which the amplitude becomes zero. Accordingly, generation of spurious frequency spectrum can be suppressed by turning ON and OFF the carrier signal by the second switch circuit 47 or the modulated signal output from the combiner 40 by a switch (not illustrated) on the time at which the amplitude becomes zero.

In Fig. 13, the first switch 32 is explained to be simply formed with the transfer switches but these switches may be formed with a wired logic circuit (not illustrated) built in the logic processing circuit 32 to provide the equivalent function to that of the switches 32.

Fig. 14 is an example of the input signal processing circuit, which has combined the logic processing circuit 35 and the serial/parallel converting circuit 34. In this figure, numeral 95 designates a circuit comprising a serial/parallel converting circuit and a read-only memory (ROM); 96 and 97, digital/analog converters; and 98 and 99, delay circuits. This circuit 95 converts the serially input baseband signal to the parallel signals and is accessed by, tow-bit preceding data, one-bit preceding data, and current data, which are all input as address signals thereto. Thus, the data read out is converted to analog phase signals by D/A converters 96 and 97.

Assuming these phase signals are cos (t) and sin (t), and the carrier wave signal as sin t, the modulated signal:

$$\sin\omega t \cos\phi(t) + \cos\omega t \sin\phi(t) = \sin\{\omega t + \phi(t)\}$$

is output from the modulating circuit 93.

Here,

$$\phi(t) = mf \cdot \sin\ \omega_s t$$

$$\omega_s = \text{bit rate}$$

$$mf = \text{modulation index}$$

Amplitude of this modulated signal does not become zero at any moment.

Fig. 15 is a block diagram of a fourth preferred embodiment of the present invention applied to a $\pi/4$ shift QPSK modulation system. In this figure, the numeral 33a designates a switch control circuit and 48, a mapping circuit. The parts like those in Fig. 13 are designated by the like numerals. The mapping circuit 48 processes the respective data of the I and Q channels from the serial/parallel converting circuit 34 and applies thus processed signals I' and Q', as vector signals carrying information of phase and amplitude, to the modulating circuit 31. Thereby, a $\pi/4$ shift QPSK signal can be obtained by the quadrature amplitude modulation in the modulating circuit 31. Such operations will be explained by referring to signal point arrangement in Fig. 16. Namely, when the input signal changes, the signal point on the I or Q axis transfers to the other signal point via the signal points on the I' and Q' axes which have been shifted by $\pi/4$-phase from the I and Q axes. For example, in case the signal is transferred to the signal point S2 from the signal point S1, the phase changes 180 degrees along the Q axis in the PSK system, therefore the modulated signal includes a large amplitude change. However, in the case of the $\pi/4$ shift QPSK system, the signal point once transfers to S1' on the Q' axis from S1 and then transfers to S2. It is also possible to transfer the signal point to S2 via a point on the I' axis. In the case of transferring to the other signal point on the I or Q axis, the signal point transfers to that on the I or Q axis via a signal point on the I' or Q' axis shifted by $\pi/4$ in phase. Therefore, the change of phase is no longer 180 degrees and the modulated signal does not have a moment at which the amplitude becomes zero. Since control is complicated for actual shift of the phase of carrier wave by $\pi/4$, this modulation system using the mapping circuit 48 equivalently processes the data as to shift by $\pi/4$. For example, in Fig. 17, the signal point S1 is equivalent to a combination of i1 and q1 on each axis I and Q. The signal point S1' on the Q' axis can be ob-

tained by providing zero component on the I' axis and providing q1+q' component on the Q' axis. Accordingly, after outputting the sum of each component i1 and q1 on the I' axis and Q' axis during the one bit period, the mapping circuit 48 outputs the q1+q' element on the Q' axis. Thereby, the signal point transfers to S2 from S1 via the signal point S2 and the phase change per each transferring does not become 180 degrees.

Fig. 18 shows a time chart for conceptionally explaining operations of the mapping circuit 48 described above. Fig. 18(a) and Fig. 18(b) respectively show the output signals of the serial/parallel converting circuit 34 in relation to the I and Q axes. The mapping circuit 48 outputs the signal for defining the signal points on the I and Q axis depending on the input data during the former half of the 1 bit period and then outputs the signal for defining the signal points on the I' and Q' axes during the latter half of the 1 bit period. As explained previously, since the $\pi/4$ shift QPSK signal does not have a zero amplitude, spurious wave is generated when the modulated signal is turned ON and OFF. Therefore, in the fourth preferred embodiment of the present invention, the modulating operation in the modulating circuit 31 is switched to the 4-phase PSK operation from the $\pi/4$ shift QPSK modulating operation by controlling the logic operations of the mapping circuit 48 by the control circuit 33a and then inputting the I and Q channel data from the serial/parallel converting circuit 34 directly to the modulating circuit 31. As explained previously, since the 100% amplitude-modulated signal is output from the combiner 40 in the 4-phase PSK operation, the second switch 47 is controlled to turn ON and OFF on such a moment that the amplitude becomes zero, or a switch (not illustrated) provided in series to the output of combiner 40 is ON/OFF-controlled in order to suppress generation of the spurious frequency spectrum.

Fig. 19 is a diagram for explaining the signal points Sa ~ Sd of the 4-phase PSK. Phase change is 180 degrees between the signal points Sa and Sc, and between the signal points Sb and Sd. Accordingly, a moment at which the amplitude becomes zero exists in the process of the 180 degree phase change. In the $\pi/4$ shift QPSK system described previously, the signal point transfers to Sc from Sa via the point Sa'. Therefore, the 180 degree phase change does not take place on a single transfer of the signal point; accordingly, then, the amplitude does not become zero. As explained above, in the fourth preferred embodiment, the modulating operation having no amplitude change of the modulated signal is at first switched to the modulating operation having 180 degree phase change by which 100% amplitude modulation takes place, and next, the modulated signal is turned OFF and ON at a moment that the amplitude becomes zero. As a result, generation of spurious frequency spectrum due to ON/OFF of the modulated signal can be suppressed. Details of the $\pi/4$-QPSK was disclosed in a report "Noncoherent Detection of $\pi/4$-QPSK System in a CCI-AWGN Combined Interference Environment" by C. C. Liu, et al. at IEEE Vehicle Technology Conference held on May 1 - 3 1989.

Fig. 20 is a diagram for explaining a fifth preferred embodiment of the present invention. The numeral 51 designates a transmitter of a base station; 52, an antenna switch; 53 and 54, antennas; 55 and 56,some of mobile stations. In an ordinal operation between the base station and the mobile stations, there is employed the offset QPSK modulation system having no moment that the amplitude becomes zero as explained above, and a diversity system is employed where the antennas 53 and 54 are switched to each other at the base station. Even in the service area of the base station, the receiving electric field may become low to deteriorate its error rate in the data communication. A mobile station suffering from such a problem issues a request to the base station to switch the antenna. Then, the base station switches the antenna under operation, for example, 53 to another antenna 54 by controlling the antenna switch 52 in accordance with the request issued from the mobile station 55. Since the base station usually communicates not only with the mobile station 55 but also with the other mobile station 56, it is necessary to make the switching momentarily between the two antennas 53 and 54. However, as explained previously, if the modulated signal is switched during the transmission thereof, the spurious frequency spectrum is generated as explained previously, interfering the other communication systems. Therefore, with an employment of one of circuits of the embodiment mentioned above, the modulating circuit of transmitter 51 is switched to the 100% amplitude modulation or to the 180 degree phase modulation, and then the antenna is switched by the switch 52 at the moment at which the amplitude of modulated signal becomes zero. Thereby, the antenna switching between 53 and 54 can be achieved without generating spurious frequency spectrum. In this case, the guard period G can be as short as 2 - 3 bit period as explained previously.

Though in the explanation in the above preferred embodiments, the modulator units 21, 22, 41, and 42 are formed, for example, with balanced mixers, it is obvious that any other types of modulator units widely used now can be employed thereto, as long as the function is satisfactorily equivalent to that of the above preferred embodiments.

Though in the above preferred embodiments it is described that interrupt/resume of the modulated wave is carried out on the moment that the amplitude becomes zero, such switching can also be done when the amplitude is not strictly zero. The timing of this switching can be determined compromisingly with the allowable level of the spurious frequency spectrum generated thereby.

The second switch referred to in the above preferred embodiments has been explained as if it is a mechanical switch, however it is also obvious that a switch circuit formed with semiconductor elements or logic cir-

cuit may be employed thereto.

The present invention is not limited only to the embodiments explained above and it may apparently be applied to the ON-OFF control of the modulated signal in the other modulation system where the amplitude of the modulated signal does not become zero.

Claims

1. A transmitter comprising:

a modulator (1) having a first mode of operation in which an amplitude of an output signal of said modulator is never substantially zero at any instant; and
second switch means (2-2) for interrupting and resuming an output signal of the modulator;

characterised in that:

said modulator is capable of one of two modes of operation depending on types of parallel input data thereto, in a second mode of the operation said output signal of said modulator being substantially 100% amplitude-modulated or substantially 180 degree phase-modulated; said transmitter comprising:
first switch means (2-1) for switching said types of the parallel input data, between a type for said first mode modulator operation and a type for said second mode modulator operation;
wherein said second switch means (2-2) is operable while said modulator is in said second mode operation; said transmitter comprising:
control means (3) for instructing said first and second switch means to operate in such manner that: after said first mode modulator operation is switched to said second mode modulation operation said output signal is interrupted on a first moment that said amplitude of said output signal becomes substantially zero, as well as, before said second mode operation is switched to said first mode operation said output signal is resumed on a second moment that said amplitude of said output signal is to become substantially zero.

2. A transmitter as recited in claim 1 further comprising an input signal processing circuit comprising:

a serial-parallel converting circuit (14,34) for converting a serial input signal to said parallel data; and
a logic processing circuit (14,35) for converting said parallel data into corresponding phase signals, each of said phase signals being input to respective one of modulation units (21,22) in said modulator, said first switch means being provided in said input signal processing circuit.

3. A transmitter as recited in claim 1, wherein said first mode operation of the modulator is an offset multiphase phase-shift keying.

4. A transmitter as recited in claim 2, wherein said logic processing circuit comprises a delay circuit (15) which delays one of said parallel signals by a half bit period, whereby said first mode of modulation mode is an offset four-phase phase-shift keying.

5. A transmitter as recited in claim 4, wherein said first switch means is a switch to disable the signal output from said delay circuit, whereby said second mode operation is a two-phase phase-shift keying.

6. A transmitter as recited in claim 4, wherein said first switch means is a switch to input one of said phase signals to both of said modulator units, whereby said second mode operation is a two-phase phase-shift keying.

7. A transmitter as recited in claim 2, wherein said logic processing circuit converts said parallel signals to analog signals each carrying frequency shift information, whereby said first mode modulator operation is a frequency shift keying.

8. A transmitter as recited in claim 7, wherein said first switch means comprises switches (32) to bypass said logic processing circuit, whereby said second mode modulator operation is a four-phase phase-shift keying.

9. A transmitter as recited in claim 2, wherein said logic processing circuit is a mapping circuit (48) which converts said parallel signals to vector signals carrying phase and amplitude information, whereby first mode modulator operation is a /4-shift quadrature phase-shift keying modulator.

10. A transmitter as recited in claim 9, wherein said first switch means bypasses said mapping circuit, whereby said second mode modulator operation is a four-phase phase-shift keying.

11. A transmitter recited in claim 1, wherein said second switch means is constituted with logic operation of said logic processing circuit.

12. A transmitter as recited in claim 1, wherein said second mode modulator operation is a four-phase phase-shift keying.

13. A transmitter as recited in claim 1, wherein said second switch means comprises a switch (27,47) pro-

vided between a local frequency oscillator and modulation units in said modulator.

14. A transmitter recited in claim 1, wherein said second switch means comprises a switch (52) provided in series to an output circuit of said modulator.

15. A transmitter as recited in claim 1, wherein said modulator comprises:

a local frequency oscillator (26);
a phase shifter (25,89) for delaying an output of said local frequency oscillator by / 2 of its phase and outputting a delayed local frequency;
a first low-pass filter (23) which is input with a first one of parallel input signals which are converted from a serial input signal to be transmitted;
a first modulator unit (21) which is input with an output of said first low-pass filter, for modulating said delayed local oscillation signal with said input signal thereto;
a second low-pass filter (24) which is input with a second one of said parallel input signals;
a second modulator unit (22) which is input with an output of said second low-pass filter, for modulating said local oscillation signal with said input signal thereto; and
a combiner (20) for summing outputs of said first modulator unit and said second modulator unit.

16. A transmitter as recited in claim 15, wherein each of said first and second modulator unit comprises a balanced mixer.

17. A method of switching operational modes of a transmitter having:

a modulator (1) capable of selective one of two modes of operations depending on types of parallel input data thereto, in a first mode of the operations an amplitude of an output signal of said modulator never being substantially zero at any instant, in a second mode of the operation said output signal of said modulator being substantially 100% amplitude-modulated or substantially 180 degree phase-modulated;
first switch means (2-1) for switching said types of the parallel input data, between a type for said first mode modulator operation and a type for said second mode modulator operation; and
second switch means (2-2) for interrupting and resuming an output signal of the modulator while said modulator is on said second mode operation,
comprising the steps of:
switching said first mode operation to said second mode operation;
interrupting said output signal on a first moment that said amplitude of said output signal becomes substantially zero;
resuming said interrupted output signal on a second moment that said amplitude of said output signal is to become substantially zero; and
switching said second mode operation to said first mode operation.

18. A method of switching antennas of a transmitting station having:

a plurality of antennas; and
a transmitter; and including the method of claim 17, wherein said interrupting step occurs on a first moment that said amplitude of said output signal becomes substantially zero;
an operational connection of said transmitter is switched from one of said antennas to another antenna;
and said resuming step occurs on a second moment that said amplitude of said output signal is to become substantially zero.

19. A transmitting station comprising:

a plurality of antennas;
a transmitter according to claim 1; and
an antenna switch for operatively connecting said transmitter to one of said antenna;
wherein said control means is for instructing said antenna switch to operate in a manner that (1) switching said first mode operation to said second mode operation; (2) interrupting said output signal on a first moment that said amplitude of said output signal becomes substantially zero; (3) switching an operational connection of said transmitter, from one of said antennas to another antenna; (4) resuming said interrupted output signal on a second moment that said amplitude of said output signal is to become substantially zero; and (5) switching said second mode operation to said first mode operation.

Patentansprüche

1. Sender, mit:

einem Modulator (1) mit einem ersten Betriebsmodus, in welchem eine Amplitude eines Ausgangssignals des Modulators niemals für einen kurzen Augenblick im wesentlichen zu Null wird; und
einer zweiten Schalteinrichtung (2-2) zum Un-

terbrechen und Wiederaufnehmen eines Ausgangssignals des Modulators;

dadurch gekennzeichnet, daß

der Modulator einen von zwei Betriebsmodi abhängig von dem Typ paralleler Eingangsdaten dazu ausführen kann, wobei das Ausgangssignal des Modulators in einem zweiten Betriebsmodus im wesentlichen zu 100% amplitudenmoduliert oder im wesentlichen 180°-phasenmoduliert ist; wobei der Sender aufweist:
eine erste Schalteinrichtung (2-1) zum Umschalten des Typs der parallelen Eingangsdaten zwischen einem Typ für den ersten Modulatorbetriebsmodus und einem Typ für den zweiten Modulatorbetriebsmodus;
wobei die zweite Schalteinrichtung (2-2) betreibbar ist, während sich der Modulator in dem Betriebsmodus befindet; wobei der Sender aufweist;
eine Steuereinrichtung (3), um den ersten und zweiten Schalter für einen Betrieb in einer solchen Weise anzuweisen, daß, nachdem der erste Modulatorbetriebsmodus auf den zweiten Modulatorbetriebsmodus umgeschaltet ist, das Ausgangssignal bei einem ersten Moment unterbrochen wird, an dem das Ausgangssignal im wesentlichen zu Null wird, sowie bevor der zweite Betriebsmodus auf den ersten Betriebsmodus umgeschaltet wird, das Ausgangssignal bei einem zweiten Moment wieder aufgenommen wird, an dem das Ausgangssignal im wesentlichen zu Null wird.

2. Sender nach Anspruch 1, welcher ferner eine Eingangssignalverarbeitungsschaltung aufweist, mit:

einer Seriell/Parallel-Wandlerschaltung (14, 34) zum Umwandeln eines seriellen Eingangssignals in die parallelen Daten; und
eine Logik-Verarbeitungsschaltung (14, 35) zum Umwandeln der parallelen Daten in entsprechende Phasensignale, wovon jedes Phasensignal in eine entsprechende Modulationseinheit (21, 22) in dem Modulator eingegeben wird, wobei die erste Schalteinrichtung in der Eingangssignalverarbeitungsschaltung vorgesehen ist.

3. Sender nach Anspruch 1, wobei der erste Betriebsmodus des Modulators eine Offset-Mehrphasen-Phasenumtastung ist.

4. Sender nach Anspruch 2, wobei die Logik-Verarbeitungsschaltung eine Verzögerungsschaltung (15) aufweist, welche eines der parallelen Signale um eine halbe Bitperiode verzögert, wodurch der erste Modus des Modulationsmodus eine Offset-4-Phasen-Phasenumtastung ist.

5. Sender nach Anspruch 4, wobei die erste Schalteinrichtung ein Schalter ist, um das von der Verzögerungsschaltung ausgegebene Signal zu unterbrechen, wodurch der zweite Betriebsmodus eine 2-Phasen-Phasenumtastung ist.

6. Sender nach Anspruch 4, wobei die erste Schalteinrichtung ein Schalter ist, um eines der Phasensignale in beide Modulatoreinheiten einzugeben, wodurch der zweite Betriebsmodus eine 2-Phasen-Phasenumtastung ist.

7. Sender nach Anspruch 2, wobei die Logik-Verarbeitungsschaltung die parallelen Signale in analoge Signale umwandelt, welche jeweils ein Frequenzverschiebungsinformation tragen, wodurch der Modulatorbetriebsmodus eine Frequenzumtastung ist.

8. Sender nach Anspruch 7, wobei die erste Schalteinrichtung Schalter (32) aufweist, um die Logik-Verarbeitungsschaltung zu umgehen, wodurch der zweite Modulatorbetriebsmodus eine 4-Phasen-Phasenumtastung ist

9. Sender nach Anspruch 2, wobei die Logik-Verarbeitungsschaltung eine Zuordnungsschaltung (48) ist, welche die parallelen Signale in Phasen- und Amplitudeninformation tragende Vektorsignale umwandelt, wodurch der erste Modulatorbetriebsmodus eine $\pi/4$-Verschiebungs-Quadraturphasenumtastung ist.

10. Sender nach Anspruch 9, wobei die erste Schalteinrichtung die Logik-Verarbeitungsschaltung umgeht, wodurch der zweite Modulatorbetriebsmodus eine 4-Phasen-Phasenumtastung ist.

11. Sender nach Anspruch 1, wobei die zweite Schalteinrichtung durch die Logikoperation der Logik-Verarbeitungsschaltung gebildet wird.

12. Sender nach Anspruch 1, wobei der zweite Modulatorbetriebsmodus einen 4-Phasen-Phasenumtastung ist.

13. Sender nach Anspruch 1, wobei die zweite Schaltereinrichtung einen Schalter (27, 47) aufweist, der zwischen einem lokalen Frequenzoszillator und Modulationseinheiten in dem Modulator vorgesehen ist.

14. Sender nach Anspruch 1, wobei die zweite Schaltereinrichtung einen Schalter (52) aufweist, welcher in Reihe mit einer Ausgangsschaltung des Modulators vorgesehen ist.

15. Sender nach Anspruch 1, wobei der Modulator aufweist:

einen lokalen Frequenzoszillator (26);
einen Phasenschieber (25, 89) zum Verzögern eines Ausgangssignals des lokalen Frequenzoszillators um $\pi/2$ seiner Phase und Ausgeben einer verzögerten lokalen Frequenz;
ein erstes Tiefpaßfilter (23), in welches ein erstes der parallelen Eingangssignale eingegeben wird, welche aus einem zu übertragenden seriellen Eingangssignal umgewandelt werden;
eine erste Modulatoreinheit (21), in welche ein Ausgangssignal des ersten Tiefpaßfilters eingegeben wird, um das verzögerte lokale Oszillationssignal mit dem darin eingegebenen Eingangssignal zu modulieren;
ein zweites Tiefpaßfilter (24), in welches ein zweites der parallelen Eingangssignale eingegeben wird;
eine zweite Modulatoreinheit (22), in welche ein Ausgangssignal des zweiten Tiefpaßfilters eingegeben wird, um das lokale Oszillationssignal mit dem darin eingegebenen Eingangssignal zu modulieren; und
einen Kombinator (20) zum Summieren der Ausgangssignale der ersten Modulatoreinheit und der zweiten Modulatoreinheit.

16. Sender nach Anspruch 15, wobei jede von der ersten und zweiten Modulatoreinheit einen symmetrischen Mischer aufweist.

17. Verfahren zum Umschalten der Betriebsmodi eines Senders, mit:

einem Modulator (1), welcher selektiv einen der zwei Betriebsmodi abhängig von dem Typ der darin eingegeben parallelen Daten ausführen kann, wobei in einem ersten Betriebsmodus eine Amplitude des Ausgangssignals niemals für ein kurzen Moment im wesentlichen zu Null wird, und in einem zweiten Betriebsmodus das Ausgangssignal des Modulators im wesentlichen zu 100% amplitudenmoduliert ist oder im wesentlichen um 180° phasenmoduliert ist;
einer ersten Schalteinrichtung (2-1) zum Umschalten des Typs der parallelen Eingangsdaten zwischen einem Typ für den ersten Modulatorbetriebsmodus und einem Typ für den zweiten Modulatorbetriebsmodus; und
einer zweiten Schalteinrichtung (2-2) zum Unterbrechen und Wiederaufnehmen eines Ausgangssignals des Modulators während sich der Modulator in dem zweiten Betriebsmodus befindet;
aufweisend die Schritte:
Umschalten des ersten Betriebsmodus auf den zweiten Betriebsmodus;
Unterbrechen des Ausgangssignals bei einem ersten Moment, bei dem die Amplitude des Ausgangssignals im wesentlichen zu Null wird;
Wiederaufnehmen des unterbrochenen Ausgangssignals bei einem zweiten Moment, bei dem die Amplitude des Ausgangssignals im wesentlichen zu Null wird; und
Umschalten des zweiten Betriebsmodus auf den ersten Betriebsmodus

18. Verfahren zum Umschalten von Antennen einer Sendestation, mit:

mehreren Antennen; und
einem Sender und einschließlich des Verfahrens nach Anspruch 17, wobei:
der Unterbrechungsschritt bei einem ersten Moment, bei dem die Amplitude des Ausgangssignals im wesentlichen zu Null wird, auftritt;
eine Betriebsverbindung des Senders von einer der Antennen aus eine andere Antenne umgeschaltet wird, und
der Wiederaufnahmeschritt bei einem zweiten Moment, bei dem die Amplitude des Ausgangssignals im wesentlichen zu Null wird, auftritt.

19. Sendestation, mit:

mehreren Antennen;
einem Sender nach Anspruch 1, und
einem Antennenumschalter, um den Sender betriebsmäßig mit einer der Antenne zu verbinden;
wobei die Steuereinrichtung dazu dient, den Antennenumschalter zu einem Betrieb in einer Weise anzuweisen, daß (1) der erste Betriebsmodus auf den zweiten Betriebsmodus umgeschaltet wird; (2) das Ausgangssignal bei einem ersten Moment unterbrochen wird, an dem die Amplitude des Ausgangssignals im wesentlichen zu Null wird; (3) ein Betriebsverbindung des Senders von einer der Antennen auf eine andere Antenne umgeschaltet wird; (4) das unterbrochene Ausgangssignal bei einem zweiten Moment wieder aufgenommen wird, an dem die Amplitude des Ausgangssignal im wesentlichen zu Null wird; und (5) der zweite Betriebsmodus auf den ersten Betriebsmodus umgeschaltet wird.

Revendications

1. Emetteur comprenant :

un modulateur (1) ayant un premier mode de

fonctionnement dans lequel l'amplitude d'un signal de sortie dudit modulateur n'est jamais sensiblement nulle à tout moment ; et,
un second moyen commutateur (2-2) pour interrompre et reprendre un signal de sortie du modulateur ;

caractérisé en ce que :

ledit modulateur peut avoir l'un de deux modes de fonctionnement selon les types des données en parallèle qui y sont entrées, dans un second mode de fonctionnement, ledit signal de sortie dudit modulateur étant modulé en amplitude sensiblement à 100 % ou étant modulé en phase sensiblement de 180 degrés ;
ledit émetteur comprenant :
un premier moyen commutateur (2-1) pour commuter lesdits types des données en parallèle d'entrée, entre un type pour ledit premier mode de fonctionnement du modulateur et un type pour ledit second mode de fonctionnement du modulateur ;
dans lequel ledit second moyen commutateur (2-2) peut être mis en fonctionnement alors que ledit modulateur est dans ledit second mode de fonctionnement ; ledit émetteur comprenant :
un moyen de commande (3) pour ordonner audits premier et second moyens commutateurs de fonctionner de manière telle que : après que ledit premier mode de fonctionnement du modulateur ait été changé en ledit second mode de fonctionnement du modulateur, ledit signal de sortie est interrompu à un premier instant où ladite amplitude dudit signal de sortie devient sensiblement nulle, ainsi que, avant que ledit second mode de fonctionnement soit changé en ledit premier mode de fonctionnement, ledit signal de sortie est repris à un second instant où ladite amplitude dudit signal de sortie doit devenir sensiblement nulle.

2. Emetteur selon la revendication 1, comprenant en outre un circuit de traitement de signaux d'entrée comprenant :

un circuit de conversion série-parallèle (14, 34) pour convertir un signal d'entrée en série en lesdites données en parallèle ; et,
un circuit de traitement logique (14, 35) pour convertir lesdites données en parallèle en signaux de phase correspondants, chacun desdits signaux de phase étant entrés dans l'une correspondante d'unités de modulation (21, 22) dans ledit modulateur, ledit premier moyen commutateur étant prévu dans ledit circuit de traitement de signaux d'entrée.

3. Emetteur selon la revendication 1, dans lequel ledit premier mode de fonctionnement du modulateur est une modulation par déplacement de phase à plusieurs phases décalées.

4. Emetteur selon la revendication 2, dans lequel ledit circuit de traitement logique comprend un circuit à retard (15) qui retarde l'un desdits signaux en parallèle d'une période d'un demi-bit, ledit premier mode de modulation étant ainsi une modulation par déplacement de phase à quatre phases décalées.

5. Emetteur selon la revendication 4, dans lequel ledit premier moyen commutateur est un commutateur pour invalider le signal sorti dudit circuit à retard, ledit second mode de fonctionnement étant ainsi une modulation par déplacement de phase à deux phases.

6. Emetteur selon la revendication 4, dans lequel ledit premier moyen commutateur est un commutateur pour entrer l'un desdits signaux de phase dans les deux dites unités de modulateur, ledit second mode de fonctionnement étant ainsi une modulation par déplacement de phase à deux phases.

7. Emetteur selon la revendication 2, dans lequel ledit circuit de traitement logique convertit lesdits signaux en parallèle en signaux analogiques portant chacun des informations de déplacement en fréquence, ledit premier mode de fonctionnement du modulateur étant ainsi une modulation par déplacement en fréquence.

8. Emetteur selon la revendication 7, dans lequel ledit premier moyen commutateur comprend des commutateurs (32) pour contourner ledit circuit de traitement logique, ledit second mode de fonctionnement du modulateur étant ainsi une modulation par déplacement de phase à quatre phases.

9. Emetteur selon la revendication 2, dans lequel ledit circuit de traitement logique est un circuit de mise en correspondance (48) qui convertit lesdits signaux en parallèle en signaux vectoriels portant des informations de phase et d'amplitude, le premier mode de fonctionnement du modulateur étant ainsi une modulation par déplacement de phase à quatre états décalés de $\pi/4$.

10. Emetteur selon la revendication 9, dans lequel ledit premier moyen commutateur contourne ledit circuit de mise en correspondance, ledit second mode de fonctionnement du modulateur étant ainsi une modulation par déplacement de phase à quatre phases.

11. Emetteur selon la revendication 1, dans lequel ledit

second moyen commutateur est constitué par une opération logique dudit circuit de traitement logique.

12. Emetteur selon la revendication 1, dans lequel ledit second mode de fonctionnement du modulateur est une modulation par déplacement de phase à quatre phases.

13. Emetteur selon la revendication 1, dans lequel ledit second moyen commutateur comprend un commutateur (27, 47) prévu entre un oscillateur de fréquence locale et des unités de modulation dans ledit modulateur.

14. Emetteur selon la revendication 1, dans lequel ledit second moyen commutateur comprend un commutateur (52) prévu en série avec un circuit de sortie dudit modulateur.

15. Emetteur selon la revendication 1, dans lequel ledit modulateur comprend :

un oscillateur de fréquence locale (26) ;
un circuit déphaseur (25,89) pour retarder en phase le signal de sortie dudit oscillateur de fréquence locale de $\pi/2$ et sortir une fréquence locale retardée ;
un premier filtre passe-bas (23) dans lequel est entré un premier des signaux d'entrée en parallèle qui sont convertis à partir d'un signal d'entrée en série à émettre ;
une première unité de modulateur (21) dans laquelle est entré le signal de sortie dudit premier filtre passe-bas, pour moduler ledit signal d'oscillation locale retardée avec ledit signal qui y est entré ;
un second filtre passe-bas (24) dans lequel est entré un deuxième desdits signaux d'entrée en parallèle ;
une seconde unité de modulateur (22) dans laquelle est entré le signal de sortie dudit second filtre passe-bas, pour moduler ledit signal d'oscillation locale avec ledit signal qui y est entré ; et,
un combineur (20) pour additionner les signaux de sortie de ladite première unité de modulateur et de ladite seconde unité de modulateur.

16. Emetteur selon la revendication 15, dans lequel chacune desdites première et seconde unités de modulateur comprend un mélangeur équilibré.

17. Procédé pour commuter les modes de fonctionnement d'un émetteur comportant :

un modulateur (1) pouvant avoir un mode sélectif parmi deux modes de fonctionnement selon les types des données d'entrée en parallèle dans celui-ci, dans un premier mode de fonctionnement l'amplitude d'un signal de sortie dudit modulateur n'étant jamais sensiblement nulle à aucun moment, dans un second mode de fonctionnement ledit signal de sortie dudit modulateur étant modulé en amplitude sensiblement à 100 % ou modulé en phase sensiblement de 180 degrés ;
un premier moyen commutateur (2-1) pour commuter lesdits types de données d'entrée en parallèle, entre un type pour ledit premier mode de fonctionnement du modulateur et un type pour ledit second mode de fonctionnement du modulateur ; et,
un second moyen commutateur (2-2) pour interrompre et reprendre un signal de sortie du modulateur alors que ledit modulateur est dans ledit second mode de fonctionnement,
comprenant les étapes qui consistent à :
changer ledit premier mode de fonctionnement en ledit second mode de fonctionnement ;
interrompre ledit signal de sortie à un premier instant où ladite amplitude dudit signal de sortie devient sensiblement nulle ;
reprendre ledit signal de sortie interrompu à un second instant où ladite amplitude dudit signal de sortie doit devenir sensiblement nulle ; et,
changer ledit second mode de fonctionnement en ledit premier mode de fonctionnement.

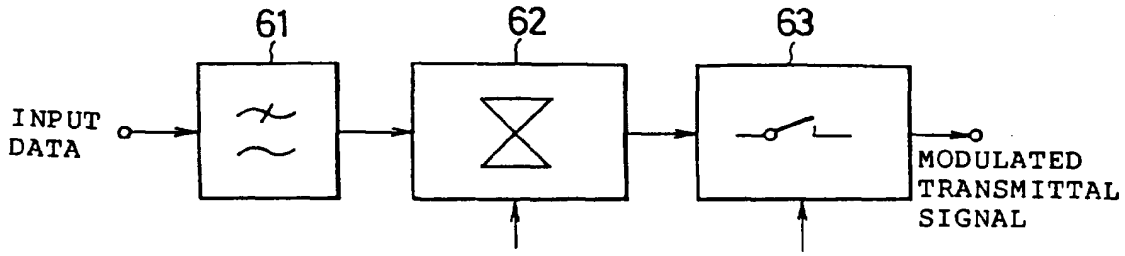
18. Procédé pour commuter des antennes d'une station d'émission comportant :

une pluralité d'antennes ; et,
un émetteur ;
et incluant le procédé selon la revendication 17, dans lequel ladite étape d'interruption a lieu à un premier instant où ladite amplitude dudit signal de sortie devient sensiblement nulle ;
une connexion active dudit émetteur est commutée de l'une desdites antennes vers une autre antenne ;
et ladite étape de reprise a lieu à un second instant où ladite amplitude dudit signal de sortie doit devenir sensiblement nulle.

19. Station d'émission comprenant :

une pluralité d'antennes ;
un émetteur selon la revendication 1 ; et,
un commutateur d'antenne pour connecter activement ledit émetteur à l'une desdites antennes ;
dans laquelle ledit moyen de commande sert à ordonner audit commutateur d'antenne de fonctionner de manière à (1) changer ledit premier mode de fonctionnement en ledit second mode de fonctionnement ; (2) interrompre ledit

signal de sortie à un premier instant où ladite amplitude dudit signal de sortie devient sensiblement nulle ; (3) commuter une connexion active dudit émetteur, de l'une desdites antennes vers une autre antenne ; (4) reprendre ledit signal de sortie interrompu à un second instant où ladite amplitude dudit signal de sortie doit devenir sensiblement nulle ; et (5) changer ledit second mode de fonctionnement en ledit premier mode de fonctionnement.



PRIOR ART FIG. 1

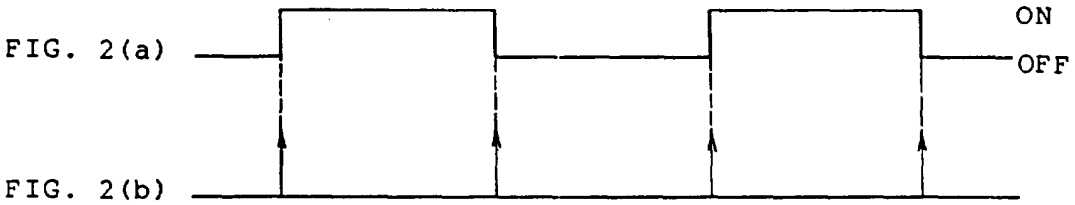


FIG. 2(a)

FIG. 2(b)

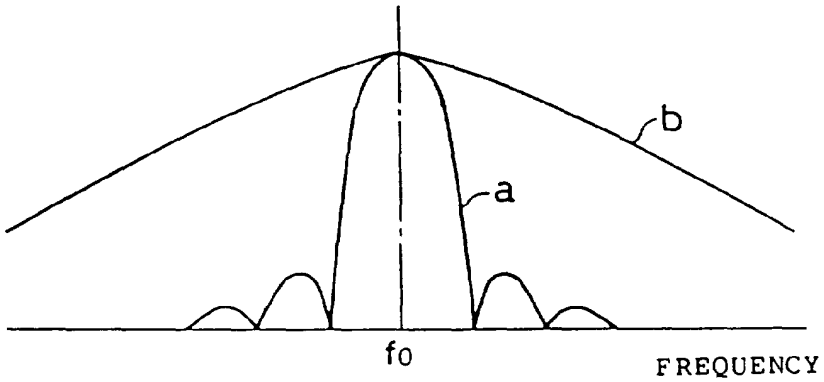
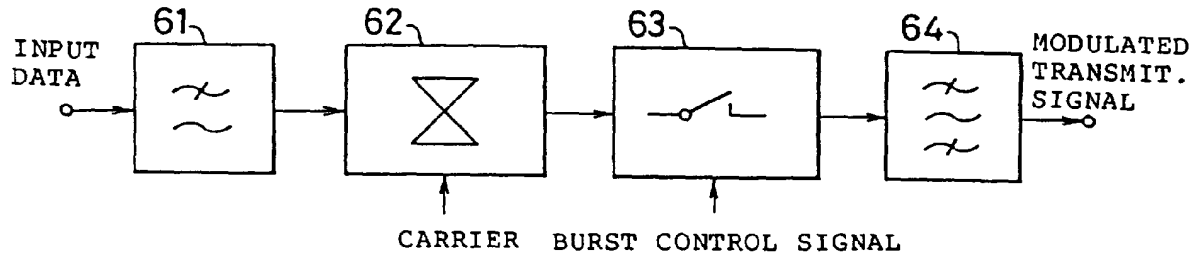
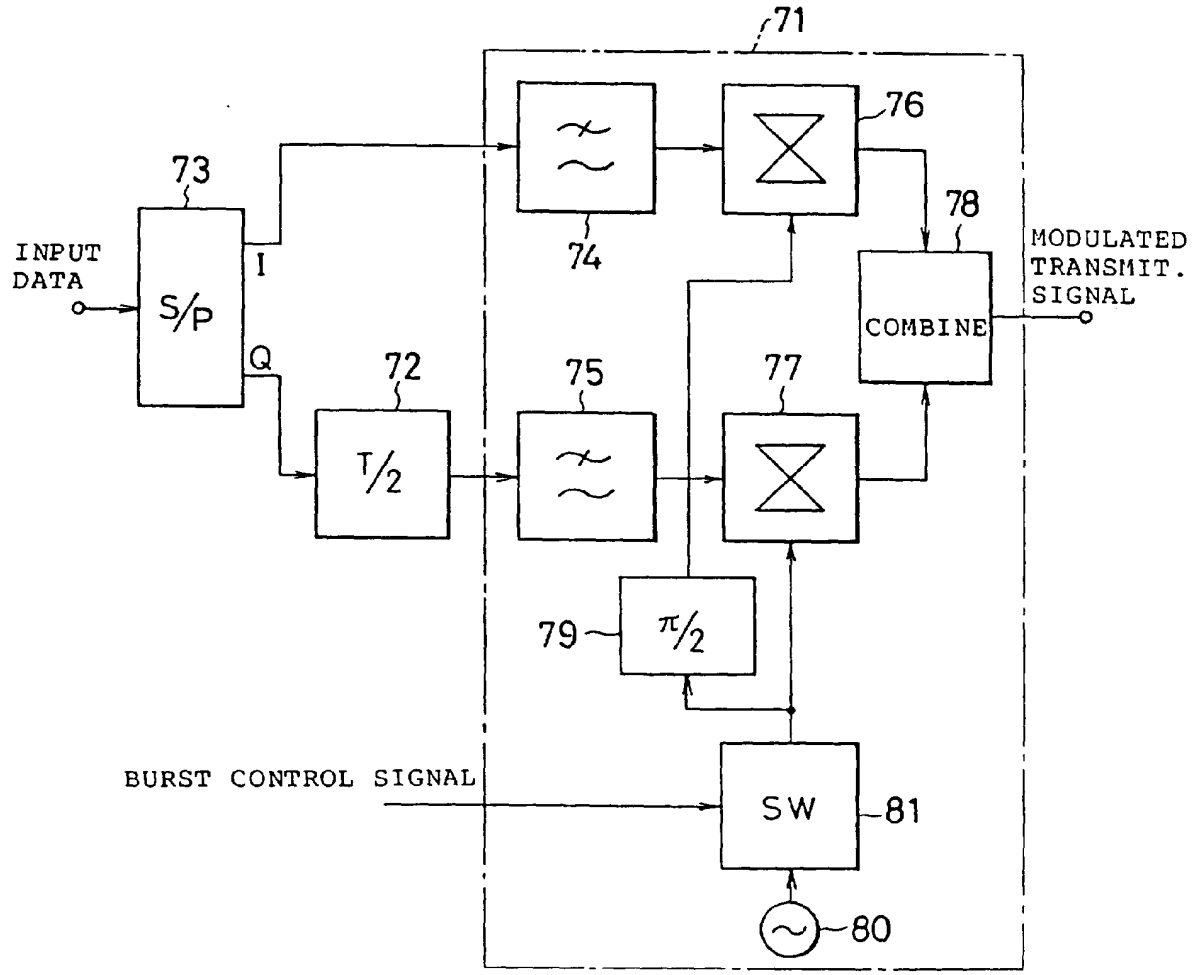


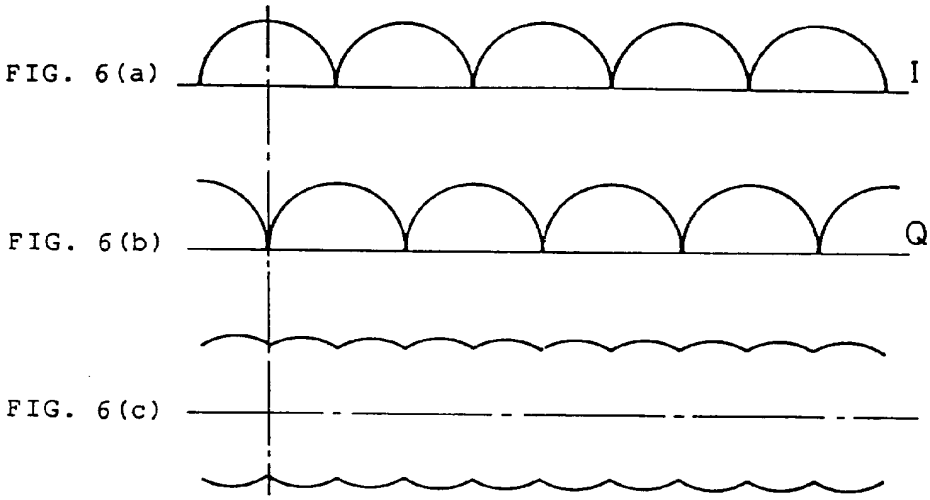
FIG. 3

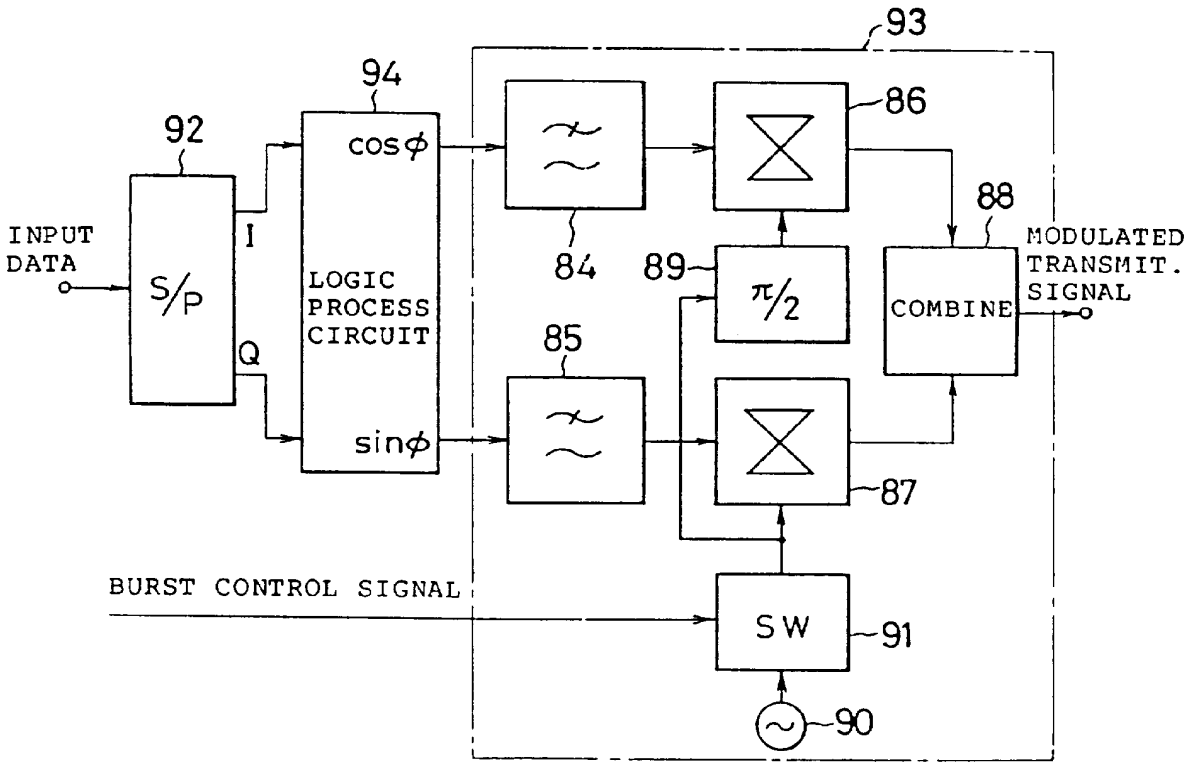


prior art FIG. 4



PRIOR ART FIG. 5





PRIOR ART FIG. 7

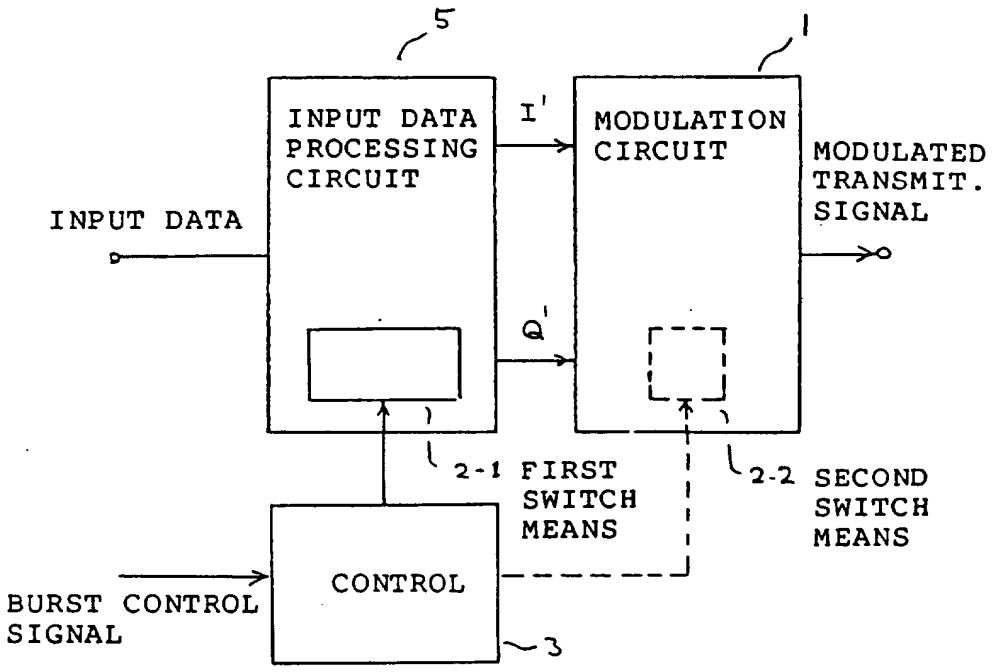

5
1
INPUT DATA PROCESSING CIRCUIT
I'
MODULATION CIRCUIT
MODULATED TRANSMIT. SIGNAL
INPUT DATA
Q'
2-1 FIRST SWITCH MEANS
2-2 SECOND SWITCH MEANS
CONTROL
BURST CONTROL SIGNAL
3

FIG. 8

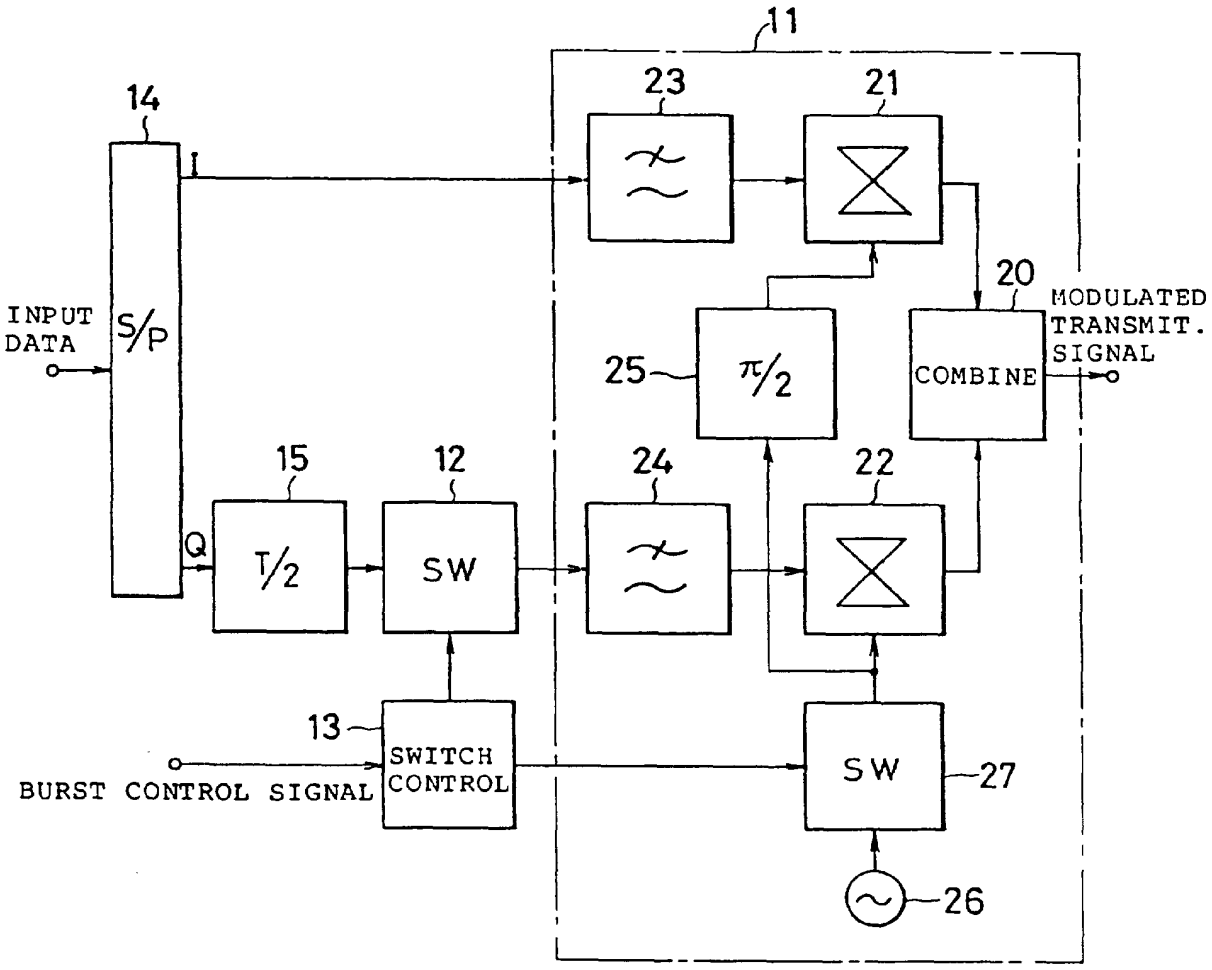
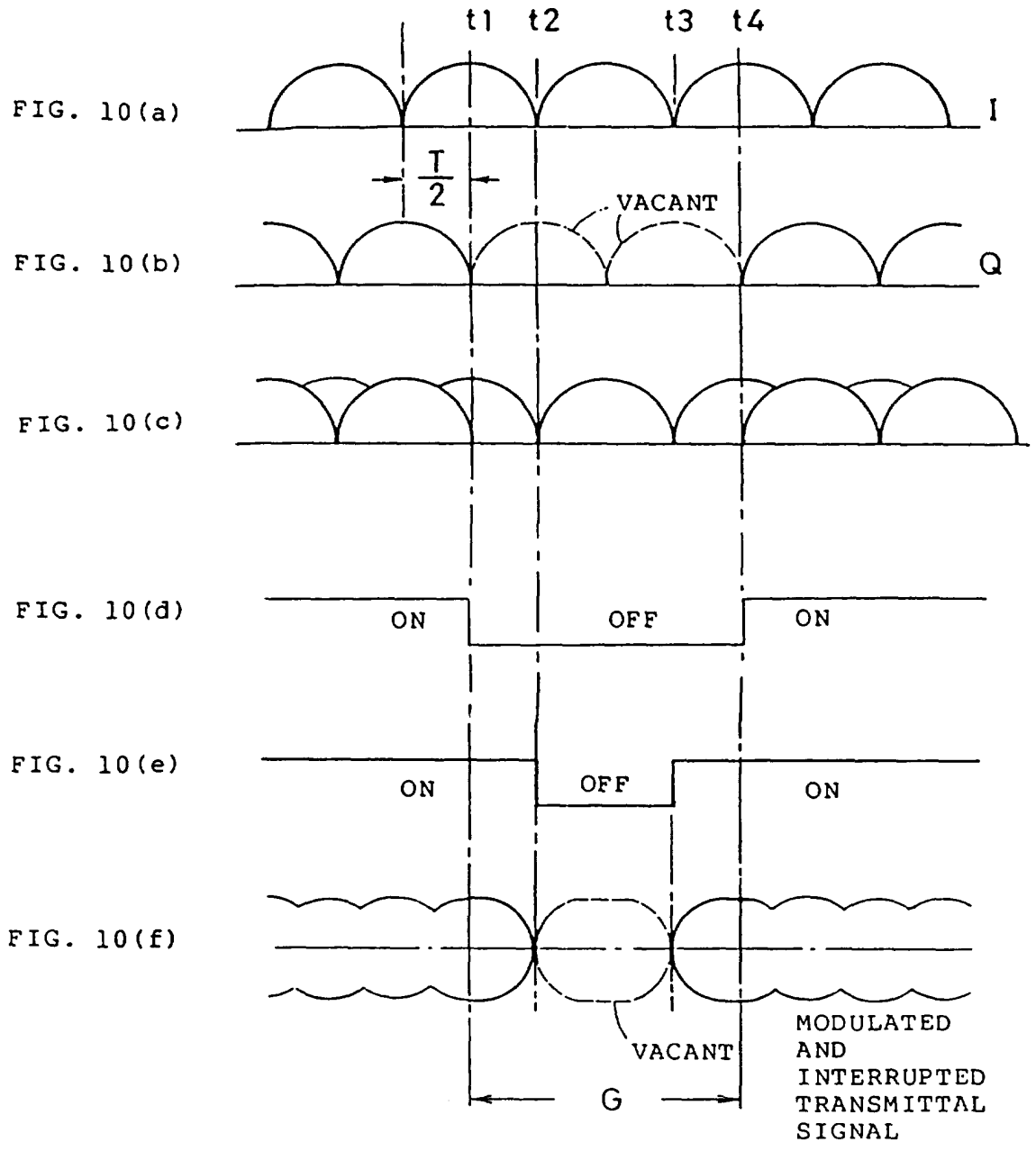

11
14
23
21
INPUT DATA
S/P
I
20
MODULATED TRANSMIT. SIGNAL
25
π/2
COMBINE
15
12
24
22
Q
T/2
SW
13
SWITCH CONTROL
BURST CONTROL SIGNAL
SW
27
26

FIG. 9


t1
t2
t3
t4
FIG. 10(a)
I
T/2
VACANT
FIG. 10(b)
Q
FIG. 10(c)
FIG. 10(d)
ON
OFF
ON
FIG. 10(e)
ON
OFF
ON
FIG. 10(f)
VACANT
G
MODULATED AND INTERRUPTED TRANSMITTAL SIGNAL

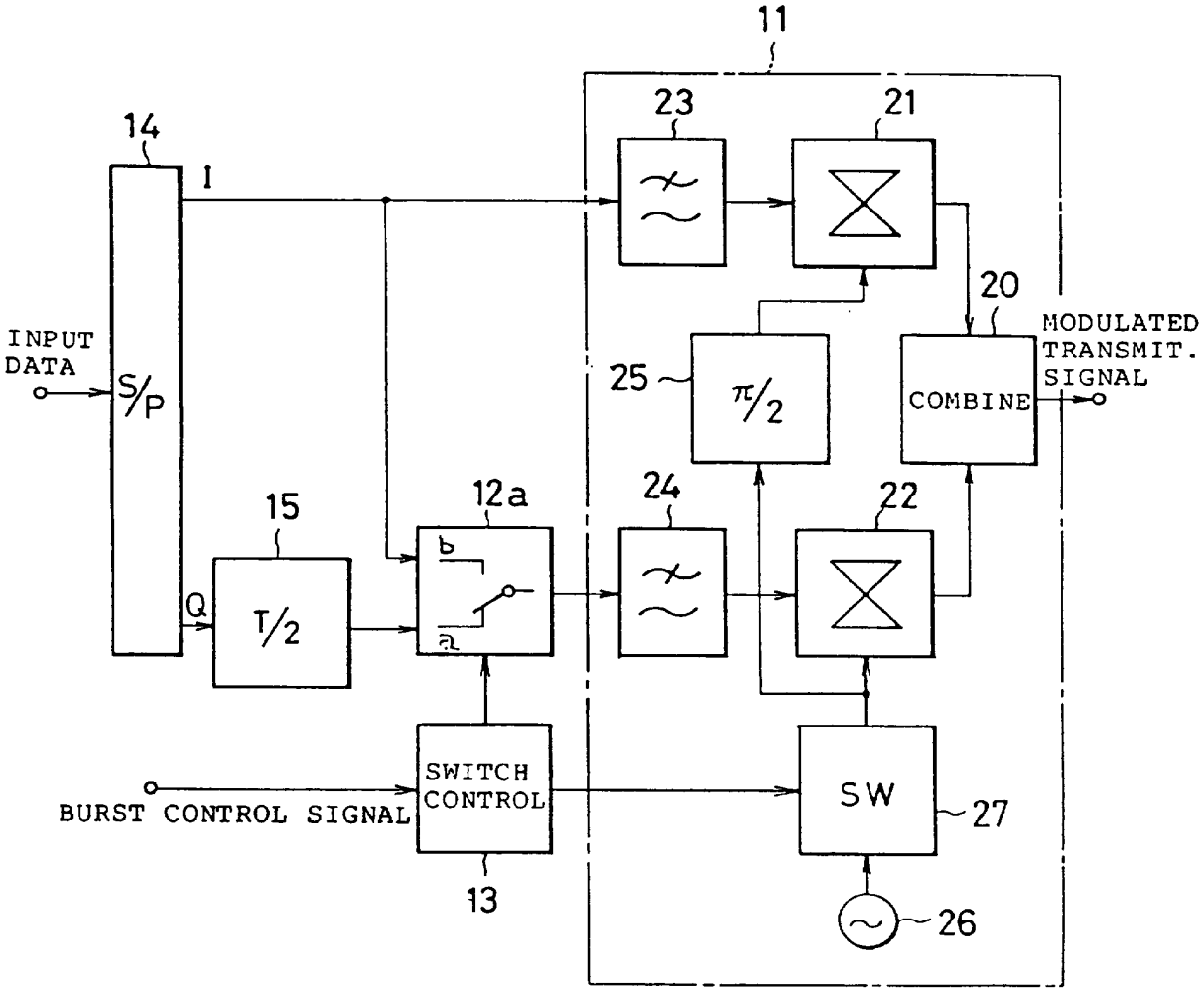

11
14
I
23
21
20
INPUT DATA
S/P
25
π/2
COMBINE
MODULATED TRANSMIT. SIGNAL
15
12a
24
22
Q
T/2
b
a
SWITCH CONTROL
SW
27
BURST CONTROL SIGNAL
13
26

FIG. 11

FIG. 12(a)

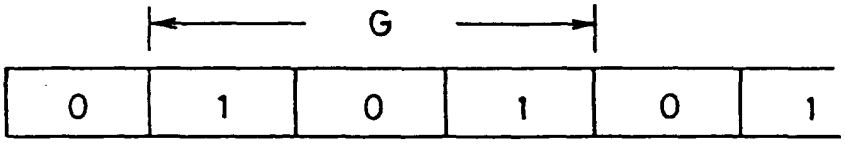


FIG. 12(b)

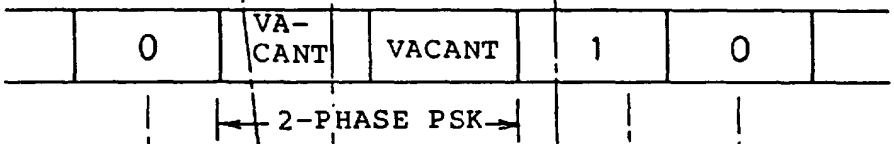


FIG. 12(c)

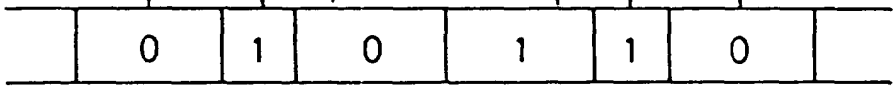
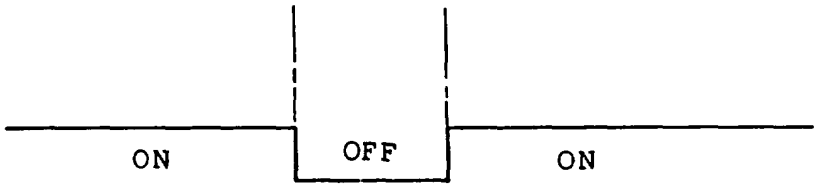


FIG. 12(d)



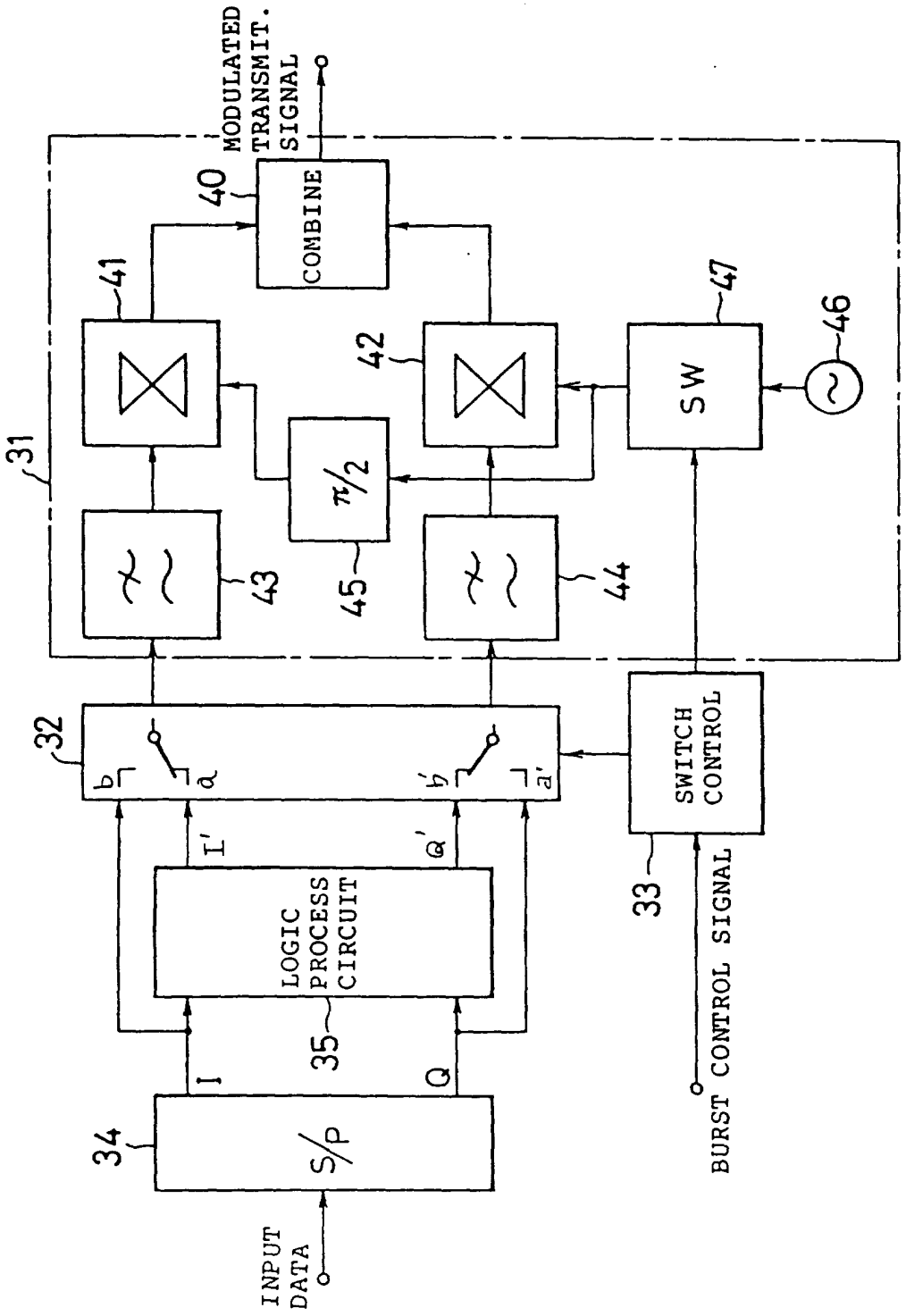

MODULATED TRANSMIT. SIGNAL
40
COMBINE
41
42
47
46
SW
31
π/2
43
45
44
32
b
a
b'
a'
SWITCH CONTROL
I'
Q'
LOGIC PROCESS CIRCUIT
35
33
I
Q
34
S/P
INPUT DATA
BURST CONTROL SIGNAL

FIG. 13

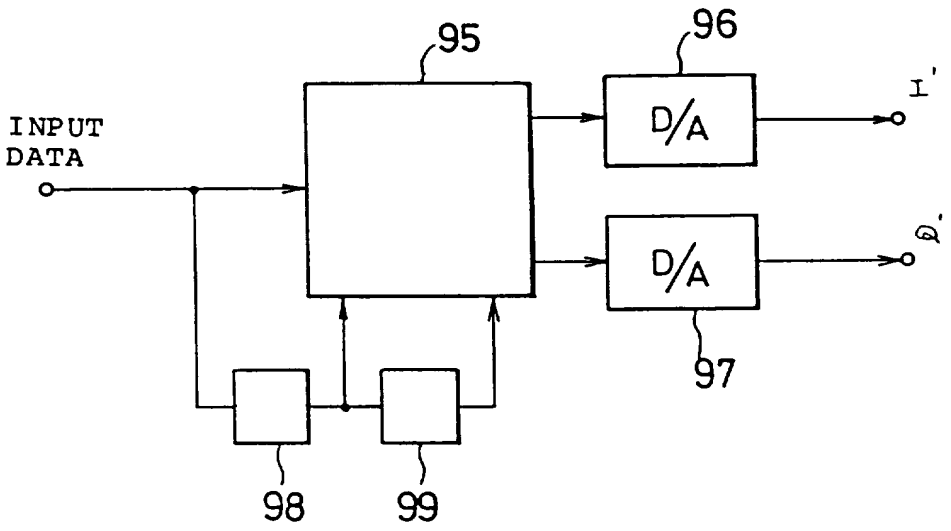


FIG. 14

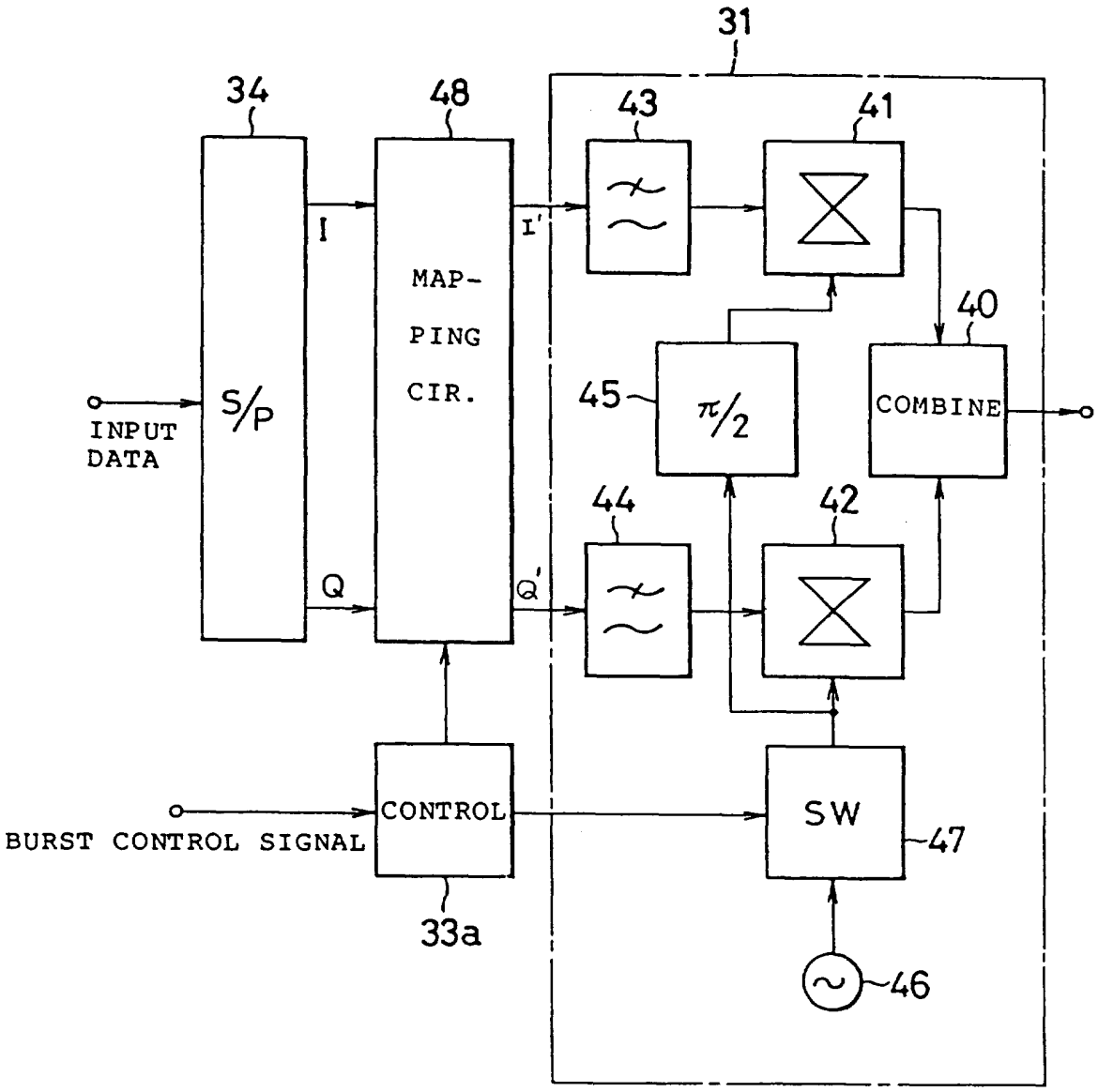

31
34
48
43
41
I
I'
MAP-
PING
CIR.
40
45
π/2
COMBINE
INPUT
DATA
S/P
44
42
Q
Q'
CONTROL
SW
47
BURST CONTROL SIGNAL
33a
46

FIG. 15

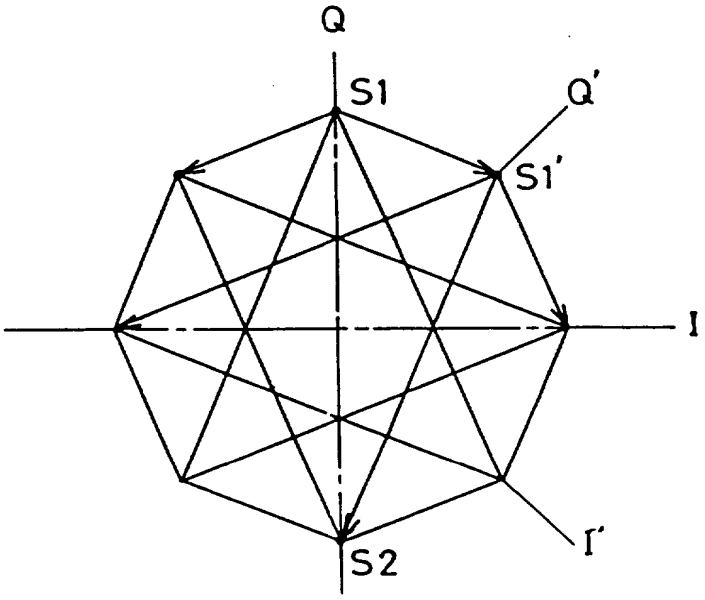


FIG. 16

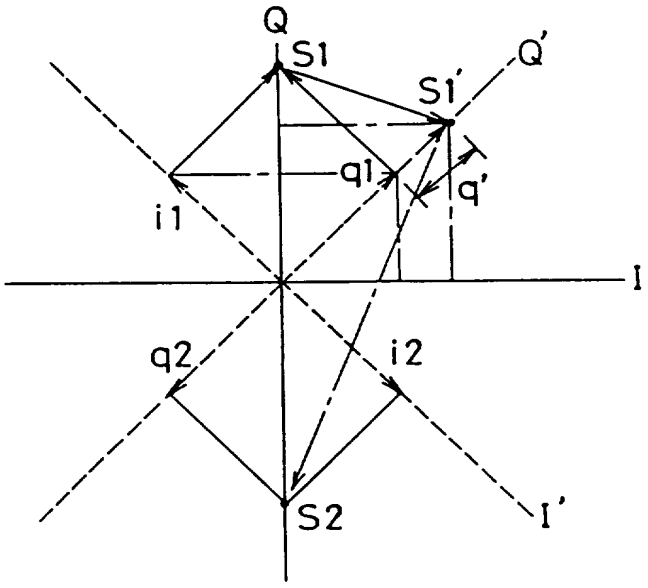


FIG. 17

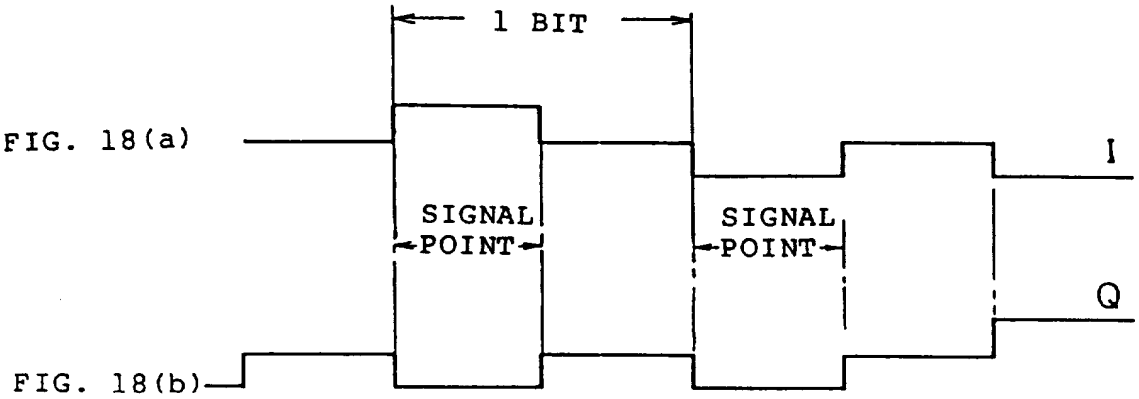

1 BIT
FIG. 18(a)
I
SIGNAL POINT
SIGNAL POINT
Q
FIG. 18(b)

FIG. 18

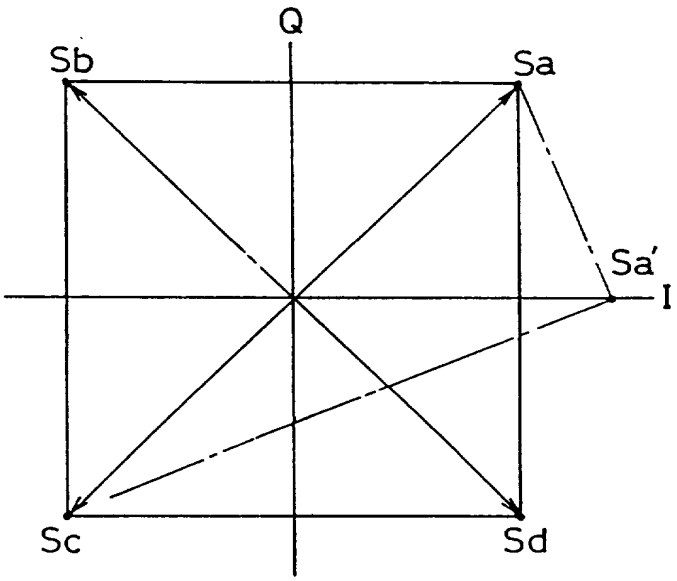

Q
Sb
Sa
Sa'
I
Sc
Sd

FIG. 19

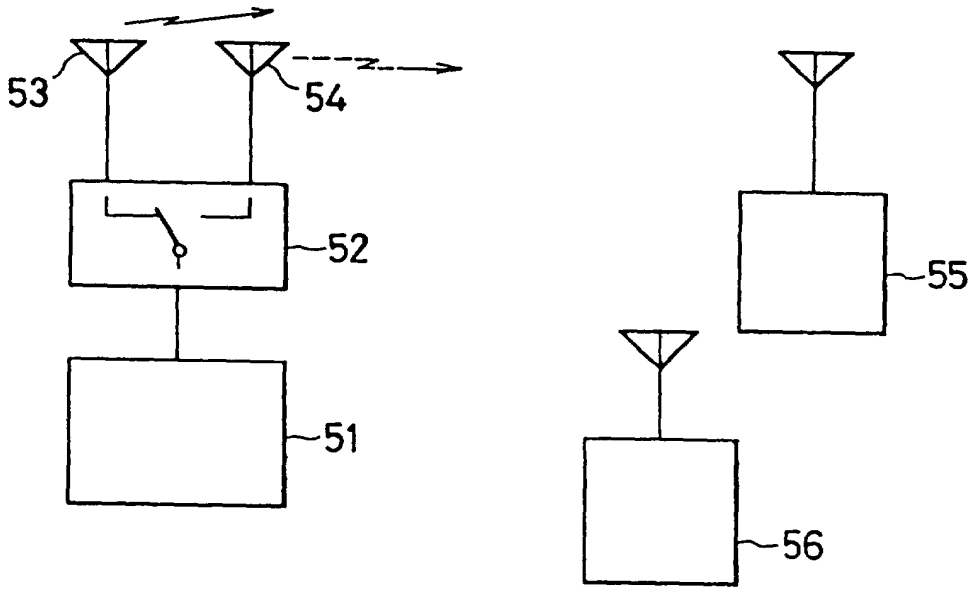


FIG. 20